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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	6

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,995	ADILETTA ET AL.	
	Examin r	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/19/01, 6/28/01 and 12/16/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Pre-Amendment A as received on 3/29/2001, Declaration as received on 6/28/2001, and Change of Address as received on 12/16/2002.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The use of the trademarks Microsoft-NT real-time, VXWorks and μCUS on page 2 of the specification has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology. Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Objections

6. Claims 1-5 and 8 are objected to because of the following informalities:

a. Claim 1 recites the limitation, "A processor, comprises" on its first line. Please amend the claim to more clearly read, "A processor, comprising." See also a similar correction on the first line of claim 5.

b. Claim 1 recites the limitation, "one of the registers" on lines 15-16 of the claim. There is no antecedent basis for this language as written. However, to the best of his ability the examiner believes that this "one of the registers" refers to the "general purpose register" or the "read transfer register" as claimed on lines 9 and 11, respectively. Please correct the claim language to read, "one of either said general purpose register or said read transfer register," in order to provide correct antecedent basis and make the claim language more clear.

c. Claims 2-4 recite the limitation, "The execution unit of claim 1" on their first lines. However, their parent claim, claim 1, is directed towards "A processor." Please correct the claim language to use the same preamble as their parent claim. For example, the examiner suggests amending the claim language to read, "The processor of claim 1, wherein said register instruction includes" for claims 2 and 3, or, "The processor of claim 1, wherein said execution unit further comprises" for claim 4.

d. Claim 8 recites the limitation, "A computer program product residing on a computer readable medium causing a processor to perform a function comprises instructions causing the processor to:" on its first and second lines. It is unclear as

claimed as to what relationships are defined (see below paragraph 12 for corresponding 112 rejection). Please correct the claim language to read more similar to, "A computer program product residing on a computer readable medium, said computer program product comprising instructions which when executed cause the processor to perform a function, the function comprising:"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-3 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites the limitation, "An execution unit for executing multiple context threads" on its second line. It is unclear whether this refers to threads having multiple contexts, or whether it refers to multiple contexts with each context being its own thread. For the purposes of the examination, the examiner will assume that the execution unit is capable of executing multiple threads, each thread being a separate context of some sort.

10. Claim 2 recites the limitation, "a bit mask specifying which one or more bytes are affected" on its second line. It is unclear what these bytes relate to. The claim language does not make clear how the bit mask specifies these unknown bytes, as the claim language as it currently is written does not provide how the bit mask determines what bytes are specified, and how in

turn those bytes are chosen from the various locations claimed. See a similar problem on the second line of claim 3.

11. Claim 2 also recites the limitation, "causing the bytes specified by the bit mask to be loaded from the immediate data bus" on its second and third lines. It is unclear where these bytes are loaded to, as no destination is specified, which makes the claim language ambiguous and indistinct. See a similar problem on lines 2-3 of claim 3.

12. Claim 8 recites the limitation, "A computer program product residing on a computer readable medium causing a processor to perform a function comprises instructions causing the processor to." It is unclear whether the function is comprised of instructions, or the computer program product comprises instructions, as well as it being unclear whether the function causes the processor to do something, or whether the instructions cause the processor to do something. For the purposes of this examination, the examiner will assume that a computer program product contains instructions, instructions that cause the processor to perform a function.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Portanova et al., U.S. Patent No. 4,992,934.

15. Regarding claim 1, Portanova has taught a processor, comprising:

a. An execution unit for executing multiple context threads, said executing unit comprising:

I. An arithmetic logic unit to process operands for executing threads (104 of Fig.3). Here, because a thread is defined as a sequential flow of instructions, the ALU (104 of Fig.3) inherently executes threads.

II. A multiplexer (124 of Fig.3),

III. Control logic to control the operation of the arithmetic logic unit and the multiplexer (30 of Fig.3),

IV. An immediate data bus coupled from the output of the control logic to an input of the multiplexer to provide immediate data to the arithmetic logic unit through the multiplexer (see Fig.3 and Col.14 lines 32-42),

V. A general-purpose register (78 of Fig.3) coupled to the input of the multiplexer to provide register operand data to the arithmetic logic unit through the multiplexer (see Fig.3 and Col.14 lines 8-17),

VI. A read transfer register (232 of Fig.3) coupled to the input of the multiplexer to provide operand data from a memory device (see Col.21 lines 50-55),

VII. Wherein execution of a register instruction causes data from one or more input sources connected to the multiplexer to be transferred through the multiplexer into the arithmetic logic unit and causes data to be transferred through the arithmetic logic unit to one of the registers (see 100 of Fig.3 and Col.14 line 52 – Col.15 line 43).

16. Regarding claim 5, Portanova has taught a method for executing multiple context threads comprising:

a. Processing operands for an executing thread through a multiplexer (124 of Fig.3) and an arithmetic logic unit (104 of Fig.3). Here, because a thread is defined as a sequential flow of instructions, the ALU (104 of Fig.3) inherently executes threads (see Col.14 lines 8-17).

b. Operating control logic (30 of Fig.3) connected to the arithmetic logic unit and the multiplexer (see Fig.3),

c. Providing immediate data on an immediate data bus coupled from the output of the control logic to an input of the multiplexer (see Fig.3 and Col.14 lines 32-42),

d. Providing operand data to the arithmetic logic unit from a general-purpose register (78 of Fig.3) coupled to the input of the multiplexer (see Fig.3 and Col.14 lines 8-17),

e. Providing operand data from a memory device through a read transfer register (232 of Fig.3) coupled to the input of the multiplexer (see Fig.3 and Col.21 lines 50-55),

f. Executing a register instruction to cause data from one or more input sources connected to the multiplexer to be transferred through the multiplexer into the arithmetic logic unit and to cause data to be transferred through the arithmetic logic unit to one of the registers (see 100 of Fig.3 and Col.14 line 52 – Col.15 line 43).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Portanova et al., U.S. Patent No. 4,992,934 as applied to claim 1 above, and further in view of Patterson et al., *Computer Organization and Design: The Hardware/Software Interface.*

19. Regarding claim 4, Portanova has taught the execution unit of claim 1, but has not explicitly taught wherein the processor further comprises:

a. A bypass bus coupled from the output of the arithmetic logic unit to an input of the multiplexer,

b. Control logic to control the execution of a series of pipelined instructions wherein each pipelined instruction may specify a read part and a write part, where the read part of one pipelined instruction specifies a read address that is the same as a write address of the write part of another pipelined instruction causing the data being written by the write part to be available to the read part in the same processor cycle.

20. However, Patterson has taught a bypass bus which connects the output of an ALU to the input of the multiplexer (see part b of Fig. 6.38). Patterson has also taught control logic (see Forwarding Unit of Fig. 6.38) which allows data that is written in one pipelined instruction to be forwarded to another instruction attempting to read that data (see Fig. 6.37) so that data hazards

can be resolved without stalling the pipeline (see p.480). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include this data forwarding logic which allows the processor to forward data from one pipeline instruction to another in order to resolve data hazards and prevent the processor from stalling.

21. Claims 2-3 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Portanova et al., U.S. Patent No. 4,992,934 as applied to claim 1 above, and further in view of the *Intel IA-64 Application Developer's Architecture Guide*.

22. Regarding claims 2 and 6, taking claim 2 as exemplary, Portanova has taught the execution unit of claim 1, but has not explicitly taught wherein the register instruction includes a bit mask specifying which one or more bytes are affected and causing the bytes specified by the bit mask to be loaded from the immediate data bus and the bytes not specified to be loaded from the read transfer register.

23. However, the *Intel IA-64 Application Developer's Architecture Guide* has taught a "mix1" instruction, which based on a bit mask selects certain bytes of data held in a first source to be loaded into a destination register, and the remaining bytes specified by the mask to be loaded from data held in a second source (see Sec. 4.6.3 of p.4-31, p.7-116 – 7-118 and p.C-21). Here, the bit mask is the opcode and the extension fields which modify the opcode in order to determine which sources, and which bytes within the sources, are selected to be loaded. One of ordinary skill in the art would have recognized that having multimedia instructions expands the functionality of a processor in a desirable way as well as improve performance (see Sec. 2.3 of p.2-2 and Sec. 4.6 of p.4-29). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include a mix1 instruction containing a bit mask

which selects bytes from a first source, the immediate data bus (see Portanova, Fig.3 and Col.14 lines 32-42), and selects the remaining bytes from a second source, the read transfer register (see Portanova, 232 of Fig.3) so that the functionality of the processor can be expanded in a useful and efficient manner and performance can be increased.

24. Claim 6 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope. Therefore, claim 6 is rejected for the same reasons as claim 2.

25. Regarding claims 3 and 7, taking claim 3 as exemplary, Portanova has taught the execution unit of claim 1, but has not explicitly taught wherein the register instruction includes a bit mask specifying which one ore more bytes are affected and causing the bytes specified by the bit mask to be loaded from the immediate data bus and the bytes not specified to be loaded from the general purpose register.

26. However, the *Intel IA-64 Application Developer's Architecture Guide* has taught a "mix1" instruction, which based on a bit mask selects certain bytes of data held in a first source to be loaded into a destination register, and the remaining bytes specified by the mask to be loaded from data held in a second source (see Sec. 4.6.3 of p.4-31, p.7-116 – 7-118 and p.C-21). Here, the bit mask is the opcode and the extension fields which modify the opcode in order to determine which sources, and which bytes within the sources, are selected to be loaded. One of ordinary skill in the art would have recognized that having multimedia instructions expands the functionality of a processor in a desirable way as well as improve performance (see Sec. 2.3 of p.2-2 and Sec. 4.6 of p.4-29). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include a mix1 instruction containing a bit mask which selects bytes from a first source, the immediate data bus (see Portanova, Fig.3 and Col.14

lines 32-42), and selects the remaining bytes from a second source, the general purpose register (see Portanova, 78 of Fig.3) so that the functionality of the processor can be expanded in a useful and efficient manner and performance can be increased.

27. Claim 7 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope. Therefore, claim 7 is rejected for the same reasons as claim 3.

28. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Portanova et al., U.S. Patent No. 4,992,934, in further in view of the *Intel IA-64 Application Developer's Architecture Guide.*

29. Regarding claim 8, Portanova has taught a computer program product residing on a computer readable medium causing a processor to perform a function comprising instructions (see Col.9 line 55 – Col.11 line 18), but has not explicitly taught wherein the instructions cause the processor to:

a. Perform a register operation which specifies a bit mask corresponding to one ore more bytes of data to cause the bytes specified by the bit mask to be loaded from an immediate data bus and the bytes not specified to be loaded from a register data bus.

30. However, the *Intel IA-64 Application Developer's Architecture Guide* has taught a "mix1" instruction, which based on a bit mask selects certain bytes of data held in a first source to be loaded into a destination register, and the remaining bytes specified by the mask to be loaded from data held in a second source (see Sec. 4.6.3 of p.4-31, p.7-116 – 7-118 and p.C-21). Here, the bit mask is the opcode and the extension fields which modify the opcode in order to determine which sources, and which bytes within the sources, are selected to be loaded. One of

ordinary skill in the art would have recognized that having multimedia instructions expands the functionality of a processor in a desirable way as well as improve performance (see Sec. 2.3 of p.2-2 and Sec. 4.6 of p.4-29). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include a mix1 instruction containing a bit mask which selects bytes from a first source, the immediate data bus (see Portanova, Fig.3 and Col.14 lines 32-42), and selects the remaining bytes from a second source, the register data bus (see Portanova, 118 of Fig.3) so that the functionality of the processor can be expanded in a useful and efficient manner and performance can be increased.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

32. Davies, U.S. Patent No. 5,450,603, has taught an SIMD parallel processor which can receive data from either of a transfer register or a source register.

33. Thayer et al., U.S. Patent No. 6,009,505, has taught the selection of various bytes from a multiple source registers to be loaded into an ALU for execution.

34. Byers et al., U.S. patent No. 5,487,159, has taught a system for processing logic operations which has the ability to choose which data is sent to an ALU from a bus received register, a general purpose register, and information from the command decode unit.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
3/18/2004

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